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1 Implementation of precise interrupts in pipelined processors

James E. Smith, Andrew R. Pleszkun
June 1985 **ACM SIGARCH Computer Architecture News , Proceedings of the 12th annual international symposium on Computer architecture ISCA '85**, Volume 13 Issue 3
Publisher: IEEE Computer Society Press, ACM Press
Full text available: pdf(893.17 KB) Additional Information: full citation, citings, index terms

2 An executable specification, analyzer and verifier for RMO (relaxed memory order)

Seungjoon Park, David L. Dill
July 1995 **Proceedings of the seventh annual ACM symposium on Parallel algorithms and architectures**
Publisher: ACM Press
Full text available: pdf(945.60 KB) Additional Information: full citation, references, citings, index terms

3 Data speculation support for a chip multiprocessor

Lance Hammond, Mark Willey, Kunle Olukotun
October 1998 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the eighth international conference on Architectural support for programming languages and operating systems ASPLOS-VIII**, Volume 32 , 33 Issue 5 , 11
Publisher: ACM Press
Full text available: pdf(1.75 MB) Additional Information: full citation, abstract, references, citings, index terms

Thread-level speculation is a technique that enables parallel execution of sequential applications on a multiprocessor. This paper describes the complete implementation of the support for threadlevel speculation on the Hydra chip multiprocessor (CMP). The support consists of a number of software speculation control handlers and modifications to the shared secondary cache memory system of the CMP This support is evaluated using five representative integer applications. Our results show that the s ...

4 Improving the performance of speculatively parallel applications on the Hydra CMP
Kunle Olukotun, Lance Hammond, Mark Willey
May 1999 **Proceedings of the 13th international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

Keywords: chip multiprocessor, data speculation, feedback-driven optimization, multithreading, parallel programming, performance evaluation

5 Cache Memories
Alan Jay Smith
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Publisher: ACM Press
Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings, index terms

6 A dynamic scheduling logic for exploiting multiple functional units in single chip multithreaded architectures
Prasad N. Golla, Eric C. Lin
February 1999 **Proceedings of the 1999 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(1.19 MB) Additional Information: full citation, references, index terms

Keywords: Tomasulo's algorithm, computer architecture, microprocessor, multithreading, threaded architectures

7 Network Protocols
Andrew S. Tanenbaum
December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4
Publisher: ACM Press
Full text available: pdf(3.37 MB) Additional Information: full citation, references, citings, index terms

8 Informing memory operations: memory performance feedback mechanisms and their applications
Mark Horowitz, Margaret Martonosi, Todd C. Mowry, Michael D. Smith
May 1998 **ACM Transactions on Computer Systems (TOCS)**, Volume 16 Issue 2
Publisher: ACM Press
Full text available: pdf(344.74 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Memory latency is an important bottleneck in system performance that cannot be adequately solved by hardware alone. Several promising software techniques have been shown to address this problem successfully in specific situations. However, the generality of these software approaches has been limited because current architecturtes do not provide a fine-grained, low-overhead mechanism for observing and reacting to memory behavior directly. To fill this need, this article proposes a new class ...

Keywords: cache miss notification, memory latency, processor architecture

9 The impact of architectural trends on operating system performance

M. Rosenblum, E. Bugnion, S. A. Herrod, E. Witchel, A. Gupta

December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95**, Volume 29 Issue 5

Publisher: ACM Press

Full text available: pdf(2.03 MB) Additional Information: full citation, references, citings, index terms

10 Informing memory operations: providing memory performance feedback in modern processors

Mark Horowitz, Margaret Martonosi, Todd C. Mowry, Michael D. Smith

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(1.55 MB) Additional Information: full citation, abstract, references, citings, index terms

Memory latency is an important bottleneck in system performance that cannot be adequately solved by hardware alone. Several promising software techniques have been shown to address this problem successfully in specific situations. However, the generality of these software approaches has been limited because current architectures do not provide a fine-grained, low-overhead mechanism for observing and reacting to memory behavior directly. To fill this need, we propose a new class of memory operati ...

11 Some formal language aspects of MARY

Mark Rain

July 1972 **ALGOL Bulletin**, Issue 34

Publisher: Computer History Museum

Full text available: pdf(1.51 MB) Additional Information: full citation, index terms

12 A programmable HIPPI interface for a graphics supercomputer

R. K. Singh, S. G. Tell, S. J. Bharrat, D. Becker, V. L. Chi

December 1993 **Proceedings of the 1993 ACM/IEEE conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(849.20 KB) Additional Information: full citation, references, citings, index terms

13 A programmable network interface for a message-based multicomputer

Raj K. Singh, Stephen G. Tell, Shaun J. Bharrat

July 1994 **ACM SIGCOMM Computer Communication Review**, Volume 24 Issue 3

Publisher: ACM Press

Full text available: pdf(814.91 KB) Additional Information: full citation, abstract, index terms

As fiber-optic gigabit networks are being deployed, supercomputer network interfaces are becoming the communication bottleneck. The Network Interface Unit (NIU) is a high-performance network interface for Pixel Planes 5, a custom, message-based multicomputer. The design offers both performance and programmability through a balance of data-handling in hardware an embedded processor. In this paper, we describe

the NIU hardware and firmware architecture. We present results of performance measuremen ...

14 Fixing the Java memory model

William Pugh

June 1999 **Proceedings of the ACM 1999 conference on Java Grande**

Publisher: ACM Press

Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

15 A comparative performance evaluation of various state maintenance mechanisms

Michael Butler, Yale Patt

December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**

Publisher: IEEE Computer Society Press

Full text available: pdf(912.33 KB) Additional Information: full citation, references, citings

16 Efficient and correct execution of parallel programs that share memory

Dennis Shasha, Marc Snir

April 1988 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 10 Issue 2

Publisher: ACM Press

Full text available: pdf(2.35 MB) Additional Information: full citation, abstract, references, citings, index terms, review

In this paper we consider an optimization problem that arises in the execution of parallel programs on shared-memory multiple-instruction-stream, multiple-data-stream (MIMD) computers. A program on such machines consists of many sequential program segments, each executed by a single processor. These segments interact as they access shared variables. Access to memory is asynchronous, and memory accesses are not necessarily executed in the order they were issued. An execution is correct if it ...

17 Operating system benchmarking in the wake of lmbench: a case study of the performance of NetBSD on the Intel x86 architecture

Aaron B. Brown, Margo I. Seltzer

June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '97**, Volume 25 Issue 1

Publisher: ACM Press

Full text available: pdf(1.98 MB) Additional Information: full citation, abstract, references, citings, index terms

The *lmbench* suite of operating system microbenchmarks provides a set of portable programs for use in cross-platform comparisons. We have augmented the *lmbench* suite to increase its flexibility and precision, and to improve its methodological and statistical operation. This enables the detailed study of interactions between the operating system and the hardware architecture. We describe modifications to *lmbench,* and then use our new benchmark suite, *hbench:OS,* to exami ...

18 A look at several memory management units, TLB-refill mechanisms, and page table organizations

Bruce L. Jacob, Trevor N. Mudge

October 1998 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the eighth international conference on Architectural**

support for programming languages and operating systems ASPLOS-VIII, Volume 32 , 33 Issue 5 , 11

Publisher: ACM Press

Full text available: pdf(1.90 MB) Additional Information: full citation, abstract, references, citings, index terms

Virtual memory is a staple in modem systems, though there is little agreement on how its functionality is to be implemented on either the hardware or software side of the interface. The myriad of design choices and incompatible hardware mechanisms suggests potential performance problems, especially since increasing numbers of systems (even embedded systems) are using memory management. A comparative study of the implementation choices in virtual memory should therefore aid system-level designers ...

19 The SimpleScalar tool set, version 2.0

Doug Burger, Todd M. Austin

June 1997 **ACM SIGARCH Computer Architecture News**, Volume 25 Issue 3

Publisher: ACM Press

Full text available: pdf(985.46 KB) Additional Information: full citation, abstract, citings, index terms

This document describes release 2.0 of the SimpleScalar tool set, a suite of free, publicly available simulation tools that offer both detailed and high-performance simulation of modern microprocessors. The new release offers more tools and capabilities, precompiled binaries, cleaner interfaces, better documentation, easier installation, improved portability, and higher performance. This paper contains a complete description of the tool set, including retrieval and installation instructions, a d ...

20 Memory consistency and event ordering in scalable shared-memory multiprocessors

Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, John Hennessy

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a

Publisher: ACM Press

Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, citings, index terms

Scalable shared-memory multiprocessors distribute memory among the processors and use scalable interconnection networks to provide high bandwidth and low latency communication. In addition, memory accesses are cached, buffered, and pipelined to bridge the gap between the slow shared memory and the fast processors. Unless carefully controlled, such architectural optimizations can cause memory accesses to be executed in an order different from what the programmer expects. The set of allowable ...

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21 Memory consistency and event ordering in scalable shared-memory multiprocessors

Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, John Hennessy

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Publisher: ACM Press

Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

22 Cost-based query scrambling for initial delays

Tolga Urhan, Michael J. Franklin, Laurent Amsaleg

June 1998 **ACM SIGMOD Record , Proceedings of the 1998 ACM SIGMOD international conference on Management of data SIGMOD '98**, Volume 27 Issue 2

Publisher: ACM Press

Full text available: pdf(1.81 MB) Additional Information: full citation, abstract, references, citings, index terms

Remote data access from disparate sources across a wide-area network such as the Internet is problematic due to the unpredictable nature of the communications medium and the lack of knowledge about the load and potential delays at remote sites. Traditional, static, query processing approaches break down in this environment because they are unable to adapt in response to unexpected delays. Query scrambling has been proposed to address this problem. Scrambling modifies query execution plans o ...

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2. **Correctly implementing value prediction in microprocessors that support multiprocessing**
Martin, M.M.K.; Sorin, D.J.; Cain, H.W.; Hill, M.D.; Lipasti, M.H.;
Microarchitecture, 2001. MICRO-34. Proceedings. 34th ACM/IEEE Internationa
1-5 Dec. 2001 Page(s):328 - 337
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3. **Value prediction in VLIW machines**
Nakra, T.; Gupta, R.; Soffa, M.L.;
Computer Architecture, 1999. Proceedings of the 26th International Symposiur
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Digital Object Identifier 10.1109/ISCA.1999.765956
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4. **Cache memories in dataflow architecture**
Kavi, K.M.; Hurson, A.R.;
Parallel and Distributed Processing, 1995. Proceedings. Seventh IEEE Sympo
25-28 Oct. 1995 Page(s):182 - 189
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Huang, I.-J.; Despain, A.M.;
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S29	6	(instruction same re$order$3) and exception and (categor$4 with dependen$4)	USPAT	OR	ON	2002/12/27 15:00
S30	18	(instruction same re$order$3) and exception and (plurality same categor$4)	USPAT	OR	ON	2002/12/27 15:01
S31	1	("6031992").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/01/20 15:19
S32	1	"5838948".PN.	USPAT	OR	OFF	2003/01/20 15:17
S33	1	"5768567".PN.	USPAT	OR	OFF	2003/01/20 15:18
S34	1	"5721927".PN.	USPAT	OR	OFF	2003/01/20 15:18
S35	1	"5574927".PN.	USPAT	OR	OFF	2003/01/20 15:18
S36	774	(micro$processor) and (instruct$3 same re$order$3) and (except$3) and (dependen$5)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:23

S37	11	(micro$processor) and (instruct$3 same re$order$3) and (except$3) and (dependen$5) and (schedul$3 with constraint$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:27
S38	12	(micro$processor) and (instruct$3 same re$order$3) and (except$3) and (dependen$5) and (schedul$3 with constrain$4)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:28
S39	30	(instruct$3 same re$order$3) and (except$3) and (dependen$5) and (schedul$3 with constrain$4)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:34
S40	0	(instruct$3 same re$order$3) and (except$3) and (dependen$5) and (schedul$3 with constrain$4) and morph$3	US-PGPUB; USPAT	OR	ON	2003/01/20 15:54
S41	9	(instruct$3 same re$order$3) and (except$3) and (dependen$5) and morph$3	US-PGPUB; USPAT	OR	ON	2003/01/20 15:56
S42	2	(instruct$3 same re$order$3) and (except$3) and (without same dependen$5) and morph$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:02
S43	10	(instruct$3 same re$order$3) and (except$3) and morph$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:02
S44	13	(instruct$3 same re$order$3) and morph$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:04
S45	16	(instruct$3 same translat$3) and (re$order$3) and morph$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:05
S46	46	(re$order$3) and (morph$3 same (host or software or code))	US-PGPUB; USPAT	OR	ON	2003/01/20 17:28
S47	1	("6031992").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/01/20 18:46
S48	100	(morph$3 with (software or host))	US-PGPUB; USPAT	OR	ON	2003/01/20 18:48
S49	17	(morph$3 with (software or host)) and (re$order$3 or re$arrang$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 18:49
S50	0	(morph$3 with (software or host)) and (intruct$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 18:49
S51	24	(morph$3 with (software or host)) and (instruct$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 18:51
S52	77	(morph$3 same (software or host)) and (instruct$3)	US-PGPUB; USPAT	OR	ON	2003/01/21 10:21
S53	16	(morph$3 same (software or host)) and (instruct$3) and (original with order$3)	US-PGPUB; USPAT	OR	ON	2003/01/21 11:05
S54	16	(morph$3 same (software or host)) and (original with order$3)	US-PGPUB; USPAT	OR	ON	2003/01/21 14:44

S55	3	(("6321272") or ("6282454") or ("6151625")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/01/21 14:44
S56	261	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3)	USPAT	OR	ON	2003/04/05 16:47
S57	278	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3)	US-PGPUB; USPAT	OR	ON	2003/04/05 16:47
S58	203	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:50
S59	181	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and (dependenc$3) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:54
S60	0	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and (probably near3 dependenc$3) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:54
S61	0	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and (probabl$2 near3 dependenc$3) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:54
S62	102	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and ((no or probably) with dependenc$3)	US-PGPUB; USPAT	OR	ON	2003/04/05 16:55
S63	0	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and ((no or probably) with dependenc$3) and "395"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:55
S64	89	(instruction near4 reorder$3) and (schedul$3) and exception and (speed or fast or improv$3) and ((no or probably) with dependenc$3) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:56
S65	2	(schedul$3 near3 microprocessor).ti.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:57
S66	7	(instruction near4 reorder$3).ti.	US-PGPUB; USPAT	OR	ON	2003/04/05 17:08
S67	1	"5941980".PN.	USPAT	OR	OFF	2003/04/05 17:04
S68	1	"5933618".PN.	USPAT	OR	OFF	2003/04/05 17:05
S69	1	"5930490".PN.	USPAT	OR	OFF	2003/04/05 17:05

S70	1	"5819057".PN.	USPAT	OR	OFF	2003/04/05 17:05
S71	1	"5778246".PN.	USPAT	OR	OFF	2003/04/05 17:06
S72	1	"5809272".PN.	USPAT	OR	OFF	2003/04/05 17:06
S73	1	"5627983".PN.	USPAT	OR	OFF	2003/04/05 17:06
S74	1	"5613080".PN.	USPAT	OR	OFF	2003/04/05 17:07
S75	1	"5560032".PN.	USPAT	OR	OFF	2003/04/05 17:07
S76	1	"5471593".PN.	USPAT	OR	OFF	2003/04/05 17:07
S77	1	"5560032".PN.	USPAT	OR	OFF	2003/04/05 17:08
S78	55	(instruction near4 (schedul$3)).ti.	US-PGPUB; USPAT	OR	ON	2003/04/05 17:09
S79	30	((instruction near4 (schedul$3)).ti.) and re$order$3	US-PGPUB; USPAT	OR	ON	2003/04/07 15:02
S80	1	"5655122".PN.	USPAT	OR	OFF	2003/04/05 17:12
S81	1	"5634023".PN.	USPAT	OR	OFF	2003/04/05 17:13
S82	1	"5627981".PN.	USPAT	OR	OFF	2003/04/05 17:15
S83	1	"5421022".PN.	USPAT	OR	OFF	2003/04/05 17:15
S84	1	"5303356".PN.	USPAT	OR	OFF	2003/04/05 17:16
S85	1	"5297281".PN.	USPAT	OR	OFF	2003/04/05 17:16
S86	1	"5269017".PN.	USPAT	OR	OFF	2003/04/05 17:17
S87	1	"5269017".PN.	USPAT	OR	OFF	2003/04/05 17:18
S88	1	"5265213".PN.	USPAT	OR	OFF	2003/04/05 17:18
S89	1	"5201057".PN.	USPAT	OR	OFF	2003/04/05 17:18
S90	1	"5201057".PN.	USPAT	OR	OFF	2003/04/05 17:18
S91	1	"5197138".PN.	USPAT	OR	OFF	2003/04/05 17:18
S92	1	("5421022").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/07 15:21
S93	69	(instruction near5 speculat$5).ti.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:22
S94	6	((instruction near5 speculat$5).ti.) and categor$3	US-PGPUB; USPAT	OR	ON	2003/04/07 15:55
S95	11	((instruction near5 speculat$5).ti.) and probabl$2	US-PGPUB; USPAT	OR	ON	2003/04/07 15:55
S96	800	adler.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:26
S97	0	michael-adler.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:24
S98	4	adler-michael.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:24
S99	0	(((instruction near5 speculat$5).ti.) and probabl$2) and "395"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:27

S100	0	(((instruction near5 speculat$5).ti.) and probabl$2) and "709"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:26
S101	0	adler.in. and "395"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:27
S102	7	adler.in. and "709"/$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:27
S103	51	mckeen.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:29
S104	21	lowney.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:50
S105	1	("6377997").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 09:52
S106	1	("5421022").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 10:30
S107	1	("5627981").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 11:14
S108	1	("5901308").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 14:11
S109	1	("5526499").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/09 10:56
S110	8	(("5421022") or ("5526499") or ("5901308") or ("5625837") or ("6065115") or ("6185668") or ("5627981") or ("5269017")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/09 10:57
S111	1	("5875340").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 11:15
S112	5	(("5467473") or ("5241633") or ("5202975") or ("5185871") or ("5590295")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 14:37
S113	1	"5261071".PN.	USPAT	OR	OFF	2003/11/13 12:37
S114	1	"5253349".PN.	USPAT	OR	OFF	2003/11/13 12:41
S115	1	"5241633".PN.	USPAT	OR	OFF	2003/11/13 12:43
S116	1	"5202975".PN.	USPAT	OR	OFF	2003/11/13 12:44
S117	1	"5185871".PN.	USPAT	OR	OFF	2003/11/13 12:44
S118	1	"5136697".PN.	USPAT	OR	OFF	2003/11/13 12:44

S119	1	"5133077".PN.	USPAT	OR	OFF	2003/11/13 12:45
S120	1	"5131086".PN.	USPAT	OR	OFF	2003/11/13 12:45
S121	1	"5051940".PN.	USPAT	OR	OFF	2003/11/13 12:46
S122	1	"4991090".PN.	USPAT	OR	OFF	2003/11/13 12:46
S123	1	"4965716".PN.	USPAT	OR	OFF	2003/11/13 12:46
S124	1	"4905200".PN.	USPAT	OR	OFF	2003/11/13 12:47
S125	1	"4831517".PN.	USPAT	OR	OFF	2003/11/13 12:47
S126	1	"4831517".PN.	USPAT	OR	OFF	2003/11/13 12:47
S127	1	"4827405".PN.	USPAT	OR	OFF	2003/11/13 12:47
S128	1	"5016208".PN.	USPAT	OR	OFF	2003/11/13 12:48
S129	1	"4977534".PN.	USPAT	OR	OFF	2003/11/13 12:49
S130	1	"4926476".PN.	USPAT	OR	OFF	2003/11/13 12:49
S131	1	"4926374".PN.	USPAT	OR	OFF	2003/11/13 12:49
S132	1	"4916696".PN.	USPAT	OR	OFF	2003/11/13 12:49
S133	1	("6594701").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 14:40
S134	1	("6347337").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 15:35
S135	1	("5958019").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/14 14:47
S136	0	("(outadj2order$3)and(eliminat$3 near3instruction)").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/14 14:48
S137	333	(out adj2 order$3) and (eliminat$3 near3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:11
S138	196	((out adj2 order$3) and (eliminat$3 near3 instruction)) and (store adj3 instruction) and (load adj3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:10

S139	5	(((out adj2 order$3) and (eliminat$3 near3 instruction)) and (store adj3 instruction) and (load adj3 instruction)) and (protect$3 adj3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 14:52
S140	5	(((out adj2 order$3) and (eliminat$3 near3 instruction)) and (store adj3 instruction) and (load adj3 instruction)) and (protect$3 adj3 register)	US-PGPUB; USPAT	OR	ON	2003/11/14 14:52
S141	8	((out adj2 order$3) and (eliminat$3 near3 instruction)) and (second near3 (store adj3 instruction)) and (second near3 (load adj3 instruction))	US-PGPUB; USPAT	OR	ON	2003/11/14 14:58
S142	184	(out adj2 order$3) and (eliminat$3 adj3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:11
S143	102	((out adj2 order$3) and (eliminat$3 adj3 instruction)) and (load adj2 instruction) and (store adj2 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:11
S144	28	(((out adj2 order$3) and (eliminat$3 adj3 instruction)) and (load adj2 instruction) and (store adj2 instruction)) and (mask)	US-PGPUB; USPAT	OR	ON	2004/05/11 16:52
S145	2	(((out adj2 order$3) and (eliminat$3 adj3 instruction)) and (load adj2 instruction) and (store adj2 instruction)) and (mask) and protect	US-PGPUB; USPAT	OR	ON	2003/11/14 15:12
S146	0	(wireless adj3 authenticat$3) and gsm and "802.11" and umts and (mobile adj3 ip)	USPAT	OR	ON	2004/05/10 19:59
S147	0	(wireless adj3 authenticat$3) and gsm and "802.11" and umts	USPAT	OR	ON	2004/05/10 19:59
S148	1	(wireless adj3 authenticat$3) and gsm and umts	USPAT	OR	ON	2004/05/10 20:00
S149	5	(wireless near3 authenticat$3) and gsm and umts	USPAT	OR	ON	2004/05/10 20:02
S150	2	(wireless near3 authenticat$3) and gsm and "802.11"	USPAT	OR	ON	2004/05/10 20:03
S151	5	(wireless near3 authenticat$3) and (mobile adj3 ip)	USPAT	OR	ON	2004/05/10 20:03
S152	6	(("6629207") or ("5751996") or ("5553256") or ("5519841") or ("6549930") or ("6453278")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:29
S153	1	("5754812").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:12

S154	1	("5799165").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:30
S155	1	("5884059").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:30
S156	1	"5517615".PN.	USPAT	OR	OFF	2004/05/11 16:50
S157	1	"5463767".PN.	USPAT	OR	OFF	2004/05/11 16:51
S158	1	"5239646".PN.	USPAT	OR	OFF	2004/05/11 16:51
S159	1	"5623628".PN.	USPAT	OR	OFF	2004/05/11 16:51
S160	1	"5317720".PN.	USPAT	OR	OFF	2004/05/11 16:51
S161	1	"5247648".PN.	USPAT	OR	OFF	2004/05/11 16:52
S162	240	((out same order$3)).ti.	US-PGPUB; USPAT	OR	ON	2004/05/11 16:53
S163	123	(((out same order$3)).ti.) and (stor$3 adj3 instruction) and (load$3 adj3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:06
S164	14	(((out same order$3)).ti.) and (stor$3 adj3 instruction) and (load$3 adj3 instruction) and (eliminat$3 adj4 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:02
S165	1	("5,737,636").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 17:02
S166	3	(((out same order$3)).ti.) and (stor$3 adj3 instruction) and (load$3 adj3 instruction) and (protect$3 near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:49
S167	72	(((out same order$3)).ti.) and (stor$3 adj3 instruction) and (load$3 adj3 instruction) and (speculat$3)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:16
S168	5	(((out same order$3)).ti.) and (stor$3 adj3 instruction) and (load$3 adj3 instruction) and (speculat$3) and (eliminat$3 near3 (load$3 or stor$3))	US-PGPUB; USPAT	OR	ON	2004/05/11 17:19
S169	6	(((out same order$3)).ti.) and (stor$3 adj3 instruction) and (load$3 adj3 instruction) and (speculat$3) and (address$3 near3 conflict$3)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:19

S170	110	(first adj4 instruction) and (second adj3 instruction) and (third adj3 instruction) and (address$3 near3 conflict$3)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:50
S171	18	(first adj4 instruction) and (second adj3 instruction) and (third adj3 instruction) and (address$3 near3 conflict$3) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/11 18:57
S172	15	(first adj4 instruction) and (second adj3 instruction) and (third adj3 instruction) and (address$3 near3 conflict$3) and (re$$order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:03
S173	1	"5517628".PN.	USPAT	OR	OFF	2004/05/11 19:00
S174	1	"5509130".PN.	USPAT	OR	OFF	2004/05/11 19:00
S175	1	"5371684".PN.	USPAT	OR	OFF	2004/05/11 19:00
S176	4	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (address$3 near3 conflict$3) and (eliminat$3 adj3 instruction) and (re$$order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:09
S177	5	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (address$3 near3 conflict$3) and (eliminat$3 adj3 instruction) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:11
S178	9	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (address$3 near3 portion) and (eliminat$3 adj3 instruction) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:13
S179	7	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (eliminat$3 adj3 instruction) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:15
S180	7	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (conflict$3 near3 instruction) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:13
S181	1	"5257354".PN.	USPAT	OR	OFF	2004/05/11 19:27
S182	50	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (reduc$4$3 near3 instruction) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:25

S183	1	("5519841").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 14:19
S184	1	("5926832").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 14:19
S185	29	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (reduc$4$3 near3 instruction) and (out$$order) and (shadow$3 near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:25
S186	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (reduc$4$3 near3 instruction) and (out$$order) and (shadow$3 near3 register) and redundan$3	US-PGPUB; USPAT	OR	ON	2004/05/12 14:26
S187	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (reduc$4$3 near3 instruction) and (out$$order) and (shadow$3 near3 register) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:26
S188	1	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (reduc$4$3 near3 instruction) and (out$$order) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:28
S189	1	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (alias near3 memory) and (out$$order) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29
S190	1	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (alias$3 near3 memory) and (out$$order) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29
S191	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (persistent near3 register) and (out$$order) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29
S192	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (instruction near3 interven$3) and (shadow near3 register) and (out$$order) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29

S193	10	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (shadow near3 register) and (out$$order) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:42
S194	4	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (access$3 near3 redundan$6)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:45
S195	6	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (eliminat$3 near3 (memory adj4 access$3))	US-PGPUB; USPAT	OR	ON	2004/05/12 14:48
S196	111	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (alias$3 near3 address)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:49
S197	17	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (alias$3 near3 operation)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:54
S198	33	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((long or short) near4 term) and flag	US-PGPUB; USPAT	OR	ON	2004/05/12 14:54
S199	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((long or short) near4 term) and flag and (alias and shadow)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:55
S200	10	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((long or short) near4 term) and flag and (shadow)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:56
S201	73	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (shadow near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:56
S202	69	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (shadow near3 register) and (long or short)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:57
S203	23	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (shadow near3 register) and (commit)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:57
S204	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (shadow near3 register) and (commit) and rollback	US-PGPUB; USPAT	OR	ON	2004/05/12 14:58

S205	23	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (shadow near3 register) and (commit)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:20
S206	0	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (shadow near3 register) and (load near3 protect$3)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:20
S207	44	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (load near3 protect$3)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:51
S208	1	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and (load near3 protect$3) and (commit or rollback)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:21
S209	270	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation))	US-PGPUB; USPAT	OR	ON	2004/05/12 15:52
S210	4	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and (protect$3 near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:55
S211	190	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and ("712"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:55
S212	81	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and protect$3 and ("712"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:56
S213	5	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and protect$3 and ("712"/$.ccls.) and (address near3 range)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:59

S214	169	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and sequenc$3 and ("712"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 16:00
S215	144	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and (sequenc$3 near3 instruction) and ("712"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 17:19
S216	42	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and (sequenc$3 near3 instruction) and ("712"/$.ccls.) and ((load$3 or stor$3) near3 protect$3)	US-PGPUB; USPAT	OR	ON	2004/05/12 16:58
S217	1	("5519841").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 17:13
S218	1	("5931957").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 17:14
S219	41	(load$3 adj4 instruction) and (stor$3 adj3 instruction) and (out$$order) and ((eliminat$3 or skip$4) near3 (instruction or operation)) and (sequenc$3 near3 instruction) and ("712"/$.ccls.) and redundan$6	US-PGPUB; USPAT	OR	ON	2004/05/12 18:20
S220	426	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:21
S221	5	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and (protect$3 near3 address)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:23
S222	25	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and (protect$3 near3 load)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:24

S223	170	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2004/05/12 18:25
S224	68	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and "712"/$.ccls. and mask$3	US-PGPUB; USPAT	OR	ON	2004/05/12 18:45
S225	85	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and ((eliminat$3 or skip$4) near3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:46
S226	57	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and ((eliminat$3) near3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:58
S227	36	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out$$order) and re$$order and ((skip$4) near3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/13 10:29
S228	1	((load or store) adj3 protect) near3 instruction	US-PGPUB; USPAT	OR	ON	2004/05/13 10:30
S229	10	((load or store) adj3 protect) near3 operation	US-PGPUB; USPAT	OR	ON	2004/05/13 13:20
S230	1	("6513110").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/02 10:36
S231	2	(("5519841") or ("5920710")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/02 11:07
S232	3	(("6011908") or ("5832205") or ("5918005")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/02 11:25
S233	1	"5689712".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:21
S234	1	"5625835".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:21

S235	1	"5542075".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:22
S236	1	"5421022".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:22
S237	1	"5420990".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:22
S238	279	(out same order$3).ti.	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/02 11:25
S239	85	(out same order$3).ti. and re$$order$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/02 11:26
S240	52	(out same order$3).ti. and re$$order$3 and stor$3 and load$3 and except$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/02 11:26
S241	781	(instruct$3 near4 schedul$3) and dependen$3 and (out near4 order$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 18:38
S242	456	(instruct$3 near4 schedul$3) and dependen$3 and (out near4 order$3) and stor$3 and load$3 and eliminat$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:38
S243	97	(instruct$3 near4 schedul$3) and dependen$3 and (out near4 order$3) and stor$3 and load$3 and (eliminat$3 near4 instruct$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 18:39
S244	68	(instruct$3 near4 schedul$3) and dependen$3 and (out near4 order$3) and stor$3 and load$3 and (eliminat$3 near4 instruct$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 18:39
S245	18	(instruct$3 near4 schedul$3) and (address$3 near4 dependen$3) and (out near4 order$3) and stor$3 and load$3 and (eliminat$3 near4 instruct$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 18:46
S246	1	("5754812").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/03 18:45
S247	52	(address$3 near4 dependen$3) and (out near4 order$3) and (stor$3 near4 load$3) and (eliminat$3 near4 instruct$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 18:46
S248	43	(address$3 near4 dependen$3) and (out near4 order$3) and (stor$3 near4 load$3) and (eliminat$3 near4 instruct$3) and (@ad<"19990614") and schedul$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:51

S249	45	(address$3 near4 dependen$3) and (re$$order$3) and (stor$3 near4 load$3) and (eliminat$3 near4 instruct$3) and (@ad<"19990614") and schedul$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:55
S250	42	(address$3 near4 dependen$3) and (re$$order$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614") and schedul$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:57
S251	37	(address$3 near4 dependen$3) and (out near4 order$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614") and schedul$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:59
S252	51	(address$3 near4 dependen$3) and (out near4 order$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:04
S253	1001	(out near4 order$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:04
S254	970	(re$order$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:05
S255	29	(re$order$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614") and (schedul$3 near4 instruct$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:08
S256	3	(re$order$3) and (eliminat$3 near4 sequenc$3) and (stor$3 and load$3) and (@ad<"19990614") and (schedul$3 near4 instruct$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:11
S257	0	(our near4 order$3) and (eliminat$3 near4 sequenc$3) and (stor$3 and load$3) and (@ad<"19990614") and (schedul$3 near4 instruct$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:11
S258	1	(our near4 order$3) and (eliminat$3 near4 sequenc$3) and (stor$3 and load$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:12
S259	1357	(eliminat$3 near4 sequenc$3) and (stor$3 and load$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:12
S260	5660	(eliminat$3 near4 operation) and (stor$3 and load$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:13

S261	645	(out near4 order$3) and (eliminat$3 near4 operation) and (stor$3 and load$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:13
S262	144	(out near4 order$3) and (eliminat$3 near4 operation) and (stor$3 and load$3) and (@ad<"19990614") and (re$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:13
S263	22	(out near4 order$3) and (eliminat$3 near4 operation) and (stor$3 and load$3) and (@ad<"19990614") and (re$order$3) and (schedul$3 near4 execut$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:14
S264	248	(out near4 order$3) and (eliminat$3 near4 operation) and (stor$3 near5 load$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:14
S265	87	(out near4 order$3) and (eliminat$3 near4 operation) and (stor$3 near5 load$3) and (@ad<"19990614") and re$order$3	US-PGPUB; USPAT	OR	ON	2005/05/03 19:14
S266	67	(out near4 order$3) and (eliminat$3 near4 operation) and (stor$3 near5 load$3) and (@ad<"19990614") and re$order$3 and schedul$3	US-PGPUB; USPAT	OR	ON	2005/05/03 19:23
S267	131	(address$3 near4 dependen$3) and (eliminat$3 near4 (instruct$3 or operation)) and (stor$3 near5 load$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:23
S268	68	(address$3 near4 dependen$3) and (eliminat$3 near4 (instruct$3 or operation)) and (stor$3 near5 load$3) and (@ad<"19990614") and (re$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:28
S269	57	(address$3 near4 dependen$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614") and (re$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/04 09:45
S270	36	(address$3 near4 dependen$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614") and (redundant)	US-PGPUB; USPAT	OR	ON	2005/05/04 09:47
S271	12	(redundant near4 instruct$3) and (eliminat$3 near4 (stor$3 or load$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/04 10:15
S272	1	"6029005".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:02

S273	1	"5797013".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:02
S274	1	"5787285".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:03
S275	1	"5751983".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:03
S276	1	"5704053".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:11
S277	1	"5555412".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:11
S278	1	"5537620".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:12
S279	1	"5526499".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:12
S280	1	"5293631".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:14
S281	104	(eliminat$3 near4 instruct$3) and (dependen$3 near4 (stor$3 or load$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/04 10:15
S282	21	(eliminat$3 near4 instruct$3) and (dependen$3 near4 (stor$3 or load$3)) and (@ad<"19990614") and re$execut$3	US-PGPUB; USPAT	OR	ON	2005/05/04 14:29
S283	1	("5519841").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/04 14:29
S284	118	(protect$3 near4 registry)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:47
S285	7	(protect$3 near4 registry) and (re$$order$3 or out$$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:51
S286	197	(protect$3 near4 register) and (re$$order$3 or out$$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:52
S287	132	(protect$3 adj4 register) and (re$$order$3 or out$$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:53
S288	111	(protect$3 adj4 register) and (re$$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:53
S289	111	(protect$3 adj4 register) and (re$$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:53
S290	4	(protect$3 adj4 register) and (re$$order$3 near4 instruct$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:57
S291	2	(protect$3 near4 (load or store) near4 register) and (re$$order$3 near4 instruct$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:58
S292	191	(protect$3 near4 (load or store) near4 register)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:58

S293	12	(protect$3 near4 (load or store) near4 register) and (re$$order$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 18:34
S294	0	("(segmentnear4identifier)andvirtual").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/13 18:35
S295	576	(segment near4 identifier) and virtual	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/13 18:35
S296	61	(segment near4 identifier) and (virtual near4 circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/13 18:37
S297	30	(segment near4 identifier) and (virtual near4 circuit) and (configur$7 near4 system)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/13 19:12
S298	1	("6513110").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 12:08
S299	319	(out near4 order$3) and (re$order$3) and (eliminat$3 near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:09
S300	258	(out near4 order$3) and (re$order$3) and (eliminat$3 near4 instruction) and (stor$3 near4 load$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:09
S301	309	(out near4 order$3) and (re$order$3) and (eliminat$3 near4 instruction) and ((stor$3 or load$3) near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:10
S302	69	(out near4 order$3) and (re$order$3) and (eliminat$3 near4 instruction) and ((stor$3 or load$3) near4 instruction) and (address$3 near4 dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:23
S303	111	(out near4 order$3) and (re$order$3) and (reduc$3 near4 instruction) and ((stor$3 or load$3) near4 instruction) and (address$3 near4 dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:23
S304	86	(out near4 order$3) and (re$order$3) and (reduc$3 near4 instruction) and ((stor$3 or load$3) near4 instruction) and (address$3 near4 dependen$3) and eliminat$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:24
S305	2	(out near4 order$3) and (re$order$3) and (reduc$3 near4 instruction) and (eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (address$3 near4 dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:25

S306	4	(out near4 order$3) and (re$order$3) and (eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (address$3 near4 dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:26
S307	5	(re$order$3) and (eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (address$3 near4 dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:28
S308	57	(re$order$3) and (eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:29
S309	48	(re$order$3) and (eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (dependen$3) and exception	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:41
S310	26	(re$order$3) and (eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (dependen$3) and exception and protect$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:30
S311	19	(eliminat$3 near4 (stor$3 or load$3) near4 instruction) and (check$3 near4 dependen$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:45
S312	124	(eliminat$3 near4 instruction) and (check$3 near4 dependen$3) and (load$3 near4 stor$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:46
S313	102	(eliminat$3 near4 instruction) and (check$3 near4 dependen$3) and ((load$3 near4 stor$3) near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:13
S314	6	(eliminat$3 near4 instruction) and (check$3 near4 dependen$3) and ((load$3 near4 stor$3) near4 protect$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:23
S315	1	(eliminat$3 near4 instruction)and ((load$3 near4 stor$3) near4 protect$3 near4 register$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:24
S316	12	(eliminat$3 near4 instruction)and ((load$3 or stor$3) near4 protect$3 near4 register$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:28
S317	29	(eliminat$3 near4 instruction)and ((load$3 or stor$3) near4 protect$3 near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:00
S318	301	(eliminat$3 near4 load$3 near4 stor$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:00
S319	93	(eliminat$3 near4 load$3 near4 stor$3) and re$$order$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:01

S320	82	(eliminat$3 near4 load$3 near4 stor$3) and re$$order$3 and exception	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:10
S321	3	(eliminat$3 near4 load$3 near4 stor$3) and re$$order$3 and exception and interferenc$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:02
S322	24	(eliminat$3 near4 load$3 near4 stor$3) and re$$order$3 and exception and re$$execut$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:13
S323	221	((load$3 or stor$3) near4 dependen$3) and (eliminat$3 near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:13
S324	31	((load$3 or stor$3) near4 dependen$3) and (eliminat$3 near4 instruction) and exception and re$$execut$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:28
S325	1	("5901308").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 15:28
S326	1	("5918005").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:33
S327	1	("6076166").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:33
S328	1	("6854370").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:34
S329	4	(("6845370") or ("5701451") or ("5727174") or ("5740362")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:34